Hybrid Memory Platform

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Outline

• The problem / The opportunity
• Project goals
• Roadmap - Sub-projects/Tracks
  • Performance Modeling
  • Hardware Prototyping
  • Heterogeneous Memory
• Industry Collaboration / Common Goals
• Summary
Moore’s Law is slowing –but the demand for cost effective capacity increases.

Cost gap between DRAM and NAND continues to increase

Need cost-effective emerging memory to fill this gap.

Sources: IDC
Big Opportunities Expected in Memory Systems:

Attachment strategies
- OpenCAPI
- DIMM Extension
- GenZ
- CCIX

Module Buffer Architectures
- DDIMM
- NVDIMM
- LRDIMM
- RDIMM

Emerging Memories
- RRAM
- MRAM
- PCM
- Flash
Mainstream Memories vs EM

* Projected information since EM is not in commercial volume production yet

<table>
<thead>
<tr>
<th></th>
<th>DRAM</th>
<th>NAND Flash</th>
<th>PCRAM</th>
<th>RRAM</th>
<th>MRAM</th>
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</thead>
<tbody>
<tr>
<td>Latency</td>
<td>++</td>
<td>-</td>
<td>-</td>
<td>+</td>
<td></td>
</tr>
<tr>
<td>Endurance</td>
<td>++</td>
<td>--</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Write Energy</td>
<td>++</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Cost per bit</td>
<td>++</td>
<td>- → + ?</td>
<td>- → + ??</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Capacity</td>
<td>+</td>
<td>- →</td>
<td>-</td>
<td>-</td>
<td></td>
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</table>

- DRAM is hard to displace due to its low latency, write energy, high endurance, and relatively low cost
- DRAM will continue as a level of hierarchy in system memory
- EM offers the promise of continued cost per bit reduction
Project Goals

• **Research**: Investigate future memory subsystem architectures around flash, emerging memories and attachment strategies. Specifically:
  • Multiple Memory types in a memory subsystem managed by hardware or software (Hybrid or Heterogeneous)
  • Multiple Memory attachment types including: Direct attach on common interface, Direct attached on unique interfaces, and Serially attached
  • Manage emerging and flash based memory to reduce cost / bit while optimizing performance in both persistent and volatile memory subsystems
  • Collaborate with industry partners to develop prototype solutions and explore the path forward for hybrid memory subsystems

Emerging Memories (RRAM, MRAM, PCM) and flash have the promise of lower cost / bit and thus could continue the $/GB improvement of memory systems
Many Emerging Memories have issues with latency, bandwidth and endurance that if unmanaged can greatly affect system performance
Hybrid memory research roadmap

3 tracks to validate ideas and quantify management impact

**Performance Modeling**
- Results to date very promising
- Challenges: slow, limited scenarios, sim assumptions

**Hardware Prototyping**
- Custom Memory board and host board development
- Run real world applications
  - POWER9 CPU
  - OpenCAPI interface

**Heterogeneous Memory**
- Trace analysis
- Data placement
- Data movement
Memory Management Options

Hardware Managed (Hybrid Memory)
- Direct Attached Management by CPU and buffers
- Serial Attached Management by Media Controller/Buffer

Software Managed (Heterogeneous Memory)
- Prototype Research
- Simulation Research

Media Controllers and Buffers:
- DDR 4/DDR 5/LPDDR 4/Flash/RRAM/MRAM/PCM
- OpenCAPI
Hybrid Memory Simulation Results

- Performance Modeling of improved EM as main memory increase cost effective capacity
- Explored Multiple configurations for DRAM + Flash/EM
- Read performance and write performance evaluated
  - Flash device modifications identified
- Endurance is an issue as expected
  - Ongoing work on evaluating solutions

### Hybrid Mem: latency

<table>
<thead>
<tr>
<th>Workload</th>
<th>DRAM</th>
<th>3DXPoint</th>
<th>No management</th>
<th>Rambus techniques</th>
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<tbody>
<tr>
<td>Data Caching</td>
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<td>20.06</td>
<td>3.10</td>
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<tr>
<td>Data Serving</td>
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<td>1.64</td>
<td>23.61</td>
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<td>Graph Analytics</td>
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<td>38.53</td>
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<tr>
<td>In-memory Analytics</td>
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<td>1.5</td>
<td>24.24</td>
<td>3.54</td>
</tr>
<tr>
<td>Media Streaming</td>
<td>1</td>
<td>1.06</td>
<td>1.55</td>
<td>1.13</td>
</tr>
<tr>
<td>Web Search</td>
<td>1</td>
<td>1.23</td>
<td>6.24</td>
<td>1.96</td>
</tr>
</tbody>
</table>

**Issue:** Poor bandwidth, latency and endurance cause performance degradation in the absence of management

**Focus:** Management policies that enable improved performance at low cost per bit

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"Performance Modeling of improved EM as main memory increase cost effective capacity"

"Explored Multiple configurations for DRAM + Flash/EM"

"Read performance and write performance evaluated"

"Flash device modifications identified"

"Endurance is an issue as expected"

"Ongoing work on evaluating solutions"
Hardware Platform for Hybrid Memory Research

• Processor
  ▪ IBM POWER9
  ▪ Joint work to develop memory subsystem for research on hybrid memory
  ▪ Demo planned in Q4 2018

• Memory
  ▪ Low latency access from OpenCAPI
  ▪ In conversation with several SCM providers
    ▪ Looking for collaboration on SCM parts, specifications, and controllers

• System
  ▪ Starting discussions with leading datacenter players
Hardware Platform for Hybrid Memory Research

- Low latency access from
  - OpenCAPI

- Memory Types
  - DDR4 DIMMs
  - Emerging Memory custom DIMMs
  - Enhanced Flash custom DIMMs
  - NVDIMM-P

- Management Policies: implemented in FPGA
Modularity for flexible and rapid experimentation

Processor

Applications and application interfaces

SW Management / policy

Interface

EM control

Drum control

Management HW / Policy

Interface control

Hybrid Controller

EM and DRAM Architecture
Potential Samsung Partnership

• Rambus Labs is looking for collaboration opportunities with key partners
• Including the use of Emerging Memories on the HW Platform to prove system benefit of DRAM and Emerging Memory
• Rambus is working to provide:
  • Hardware research platform access
  • Benchmarking
  • Management policies/algorithms
# Common Research Goals Hybrid

<table>
<thead>
<tr>
<th>Rambus</th>
<th>Processor Leaders</th>
<th>Memory Leaders</th>
<th>System Leaders</th>
</tr>
</thead>
</table>
| • Study IS protocols (OpenCAPI)  
• Study any emerging memory and hybrid  
• Run real world applications  
• Study Serial vs direct attach | • Programming models  
• Resource sharing / partitioning / provisioning  
• Interface comparisons | • Analysis of EM types  
• Demo Emerging Memories  
• Estimate direct attach performance  
• Real world application testing | • Functional testing of IS Protocols (OpenCAPI)  
• Functional testing of NVDIMM  
• Designs that can be modified to be a product |
THANK YOU